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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,456	07/17/2003	Chin Lee	4444-0120P	9179

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EXAMINER	
CONTINO, PAUL F	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 12/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,456	LEE, CHIN	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to under 37 CFR 1.71, as being so incomprehensible as to preclude a reasonable search of the prior art by the examiner. For example, the following items are not understood:

As in the Applicant's Specification on pages 4 in lines 12-15 and on page 7 lines 4-7, the disclosure of the compare circuit writing data to memories is interpreted as not being enabled (see Figures 1A, 1B, and 2A). It is interpreted that the only component, as disclosed throughout the Specification, as being able to write to memories is the control circuit, as depicted in Figure 1A and described on page 3 in lines 20-24.

2. Applicant is required to submit an amendment which clarifies the disclosure so that the examiner may make a proper comparison of the invention with the prior art.

Applicant should be careful not to introduce any new matter into the disclosure (i.e., matter which is not supported by the disclosure as originally filed).

Claim Objections

3. Claim 14 is objected to because of the following informalities: line 3 states the term "repair" where "repairs" is more correct. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 9 and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention..

As in claims 9 and 18, the limitations reciting a compare circuit as writing to the plurality of memories is interpreted as not being enabled.

* * *

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 2-9 and 11-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2-9 and 11-18 recite the limitation "[t]he circuit" in line 1. There is insufficient antecedent basis for this limitation in the claim. There are three circuits disclosed in independent base claims 1 and 10, respectively: a memory modeling circuit, a compare circuit, and a control circuit. In order to apply prior art, the Examiner has interpreted "the circuit" as the "memory modeling circuit".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 3, 4, 5, 7, 8, 10, 11, 12, 13, 15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kiso et al. (U.S. Patent No. 5,757,809).

As in claim 1, Kiso et al. discloses a memory modeling circuit with fault toleration, comprising:

a compare circuit, comparing data stored in the same address of a plurality of memories *(Fig. 3, Pattern comparing circuit C; column 5 lines 41-43 and 46-53, which disclose the same address in a plurality of memories; and column 5 line 65 through column 6 line 3, which discloses a comparison of the data)*; and

a control circuit coupled to said plurality of memories, wherein said control circuit controls said data to be read or written from/to said plurality of memories *(Fig.3, the combination of Bin, Bout, J, and TM; columns 4-6)*.

As in claim 2, Kiso et al. discloses a test circuit, receiving said data and the reading data generated by said compare circuit to generate a testing result *(Fig. 3, the combination of Bout and J; column 6 lines 1-20)*.

As in claim 3, Kiso et al. discloses said test circuit further comprises a plurality of sub-test circuits with the same circuit design *(Fig. 4; column 5 lines 10-12, where the transistors of Bout are interpreted as sub-test circuits with a same circuit design)*.

As in claim 4, Kiso et al. discloses said testing result gets an error code and then a faulty memory or a faulty sub-test circuit can be identified according to said error code *(column 6 lines 4-24, where the disagreement signal is interpreted as an error code)*.

As in claim 5, Kiso et al. discloses said plurality of memories are the same type of memory *(column 4 lines 41-45, where it is interpreted that the memory cell arrays are of the same type of memory)*.

As in claim 7, Kiso et al. discloses said compare circuit further comprises a plurality of sub-compare circuits with the same circuit design *(Fig. 2, AND gates; column 1 lines 42-43)*.

As in claim 8, Kiso et al. discloses said control circuit stops receiving the data sent from said compare circuit until said control circuit enters the reading mode while said control circuit is in the writing mode *(Fig. 3; column 5 line 44 through column 6 line 1, where it is interpreted that the transfer gates are open only during reads and writes, which occur at different times than one another)*.

As in claim 10, Kiso et al. discloses a memory modeling circuit with fault toleration, comprising:

a compare circuit receiving data stored in the same address of a plurality of memories and comparing the data with each other *(Fig. 3, Pattern comparing circuit C; column 5 lines 41-43 and 46-53, which disclose the same address in a plurality of memories; and column 5 line 65 through column 6 line 3, which discloses a comparison of the data)*;

a control circuit connecting said plurality of memories, wherein said control circuit enters a writing mode and writes data to the same address of said plurality of memories, and said control circuit enters a reading mode to load data generated by said compare circuit *(Fig.3, the combination of Bin, Bout, J, and TM; columns 4-6)*; and

a test circuit receiving the data stored in the same address of said plurality of memories and the data generated by said compare circuit to generate a testing result *(Fig. 3, the combination of Bout and J; column 6 lines 1-20)*.

As in claim 11, Kiso et al. discloses said test circuit further comprises a plurality of sub-test circuits with the same circuit design *(Fig. 4; column 5 lines 10-12, where the transistors of Bout are interpreted as sub-test circuits with a same circuit design)*.

As in claim 12, Kiso et al. discloses said testing result can identify a faulty memory or a faulty sub-test circuit *(column 6 lines 23-24)*.

As in claim 13, Kiso et al. discloses said compare circuit further comprises a plurality of sub-compare circuits with the same circuit design *(Fig. 2, AND gates; column 1 lines 42-43)*.

As in claim 15, Kiso et al. discloses said plurality of memories are the same type of memory *(column 4 lines 41-45, where it is interpreted that the memory cell arrays are of the same type of memory)*.

As in claim 17, Kiso et al. discloses said control circuit stops receiving data sent from said compare circuit until said control circuit enters the reading mode while said control circuit is in the writing mode *(Fig. 3; column 5 line 44 through column 6 line 1, where it is interpreted that the transfer gates are open only during reads and writes, which occur at different times than one another)*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiso et al. in view of Roohparvar (U.S. Patent No. 7,047,455).

As in claims 6 and 16, Kiso et al. teaches of RAM memory *(column 4 line 40)*. However, Kiso et al. fails to teach of SDRAM. Roohparvar teaches of SDRAM *(column 6 lines 61-65, where an SDRAM interface implies SDRAM)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the SDRAM as taught by Roohparvar in the invention of Kiso et al. This would have been obvious because the invention of Roohparvar teaches of SDRAM, which allows for storing of information when power is off so as not to lose data *(column 1 lines 21-27)*, in a memory testing environment exhibiting fault tolerance.

* * *

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kiso et al. in view of Ricchetti et al. (U.S. Patent No. 6,957,371).

As in claim 14, Kiso et al. teaches of an error code. However, Kiso et al. fails to teach of an engineer and repair. Ricchetti et al. teaches that a testing result gets an error code and then an engineer knows the fault part according to different error code combinations and repair said fault part to keep the reliability *(column 14 lines 43-49 and column 15 lines 32-33, where a user is interpreted as an engineer)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the engineer and repair as taught by Ricchetti et al. in the invention of Kiso et al. This would have been obvious because communicating fault information corresponding to a particular component to a user allows in order to repair a system, as taught by Ricchetti et al., increases the overall ability for a computer system to continue functioning properly and safely.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent 7,137,050 Merritt et al. discloses multiple memories with data comparison.

U.S. Patent 4,628,509 Kawaguchi discloses testing of redundant memory.

U.S. PGPub 2003/0204797 Lin discloses parallel memory tests.

U.S. Patent 7,013,414 Takeshige et al. discloses multiple RAMs under test.

U.S. Patent 6,009,026 Tamlyn et al. discloses multiple RAM under test.

JP 06150698 A discloses same addressing of multiple memories under test.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PFC
11/29/2006

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER